

Technical Notes on using Analog Devices' DSP components and development tools

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ADSP-218x Full Memory Mode vs. Host Memory Mode (2184, 2184L, 2185, 2185L, 2185M, 2186, 2186L, 2186M, 2187L, 2188M, 2189M)

Last Modified: 1/14/96

Overview

There are two major configurations for the external busses on the ADSP-218x DSPs that define the types of memory accesses that can be performed on these devices. The two modes of operation are described below:

I/O Modes of Operation

- **Full Memory Mode:** Gives complete use of the external address and data busses as found in the ADSP-2181. Allows BDMA operation with full external overlay memory and I/O capability. IDMA functionality disabled
- **Host Mode:** Allows complete IDMA port operation with limited external addressing capabilities. (Mode C = 1)

Mode C Pin: The two operating modes defined above are determined by the state of the Mode C pin during /RESET and cannot be changed once the DSP is powered up and execution begins. For information on setting the Mode C pin for passive or active configuration, refer to the ADSP-218x data sheet.

Full Memory Mode

Full Memory Mode gives complete use of the external address and data busses as found in the

ADSP-2181. In Full Memory Mode, the ADSP-218x behaves like an ADSP-2181 with the IDMA port removed. There is a 24 bit external data bus, a 14 bit address bus and 5 memory select signals. Byte memory is accessed using the middle eight bits of the data bus for data. The upper eight bits of the data bus together with the 14 address pins provide a 22 bit address for byte memory space. All of these features behave exactly the same as on the ADSP-2181. Hold Off cases (autobuffer cycle stealing, external memory accesses with wait states, etc..) are simplified because an IDMA transfer will never occur. In this mode the IDMA port is disabled as if /IS was deselected or pulled high on the ADSP-2181.

Host Mode

Host Mode gives full use of the IDMA port as found on the ADSP-2181, but there are limitations on the use of the external memory bus. In Host Mode the lower eight bits of the data bus, D[7:0] become IDMA control pins and IAD bus pins. The upper 13 bits of the address bus A[13:1] become the lower 13 bits of the IDMA address/data bus, IAD[12:0]. The Pinout Diagram and tables for the Memory Interface Pins in the ADSP-218x Data Sheets show the alternate functions for each pin in either major I/O mode. IDMA transfers occur exactly as on the ADSP-2181.

Accessing Peripherals

The external bus in Host Mode still remains available in a limited form. The DSP's address pins A[13:1] are changed to IAD[12:0] when the Mode C pin is high. As a result, the chip cannot drive an address externally. However, internally the chip will behave as if external accesses are occurring. The external bus will behave as an ADSP-2181 system where address bits A[13:1] and data bits D[7:0] are ignored. The upper 16 bits of

the data bus can still be used for external data transfers, but only on address bit is available, A0. Writes to Data Memory or I/O Space will activate the appropriate memory select(s), /RD or /WR, place data on D[23:8], and drive a single address bit on A0. Program memory reads and writes behave similarly but have the added consideration of the PX register. For program memory reads and writes only the upper 16 bits will be available externally. When 24 bit data is written to external program memory the upper 16 bits will be driven out on data bus pins [23:16]. The PX register will still latch the lower eight bits of the program memory word, but they will not be driven externally. If a 24 bit read of external memory occurs no external pins will control the value of the PX register, and the PX register will be written with all ones.

The missing address bits restrict using the external bus with a conventional memory device which has separated address and data buses. These external transfers might be usable with shared address/data memory chips or can be used for communication with an ASIC. The memory selects will still be active, so each memory space is effectively collapsed into two external addresses, address 0 and 1. Clever use of the /CMS pin will allow a user to decode 8 external addresses of 16 bit words using A0, /IOMS, /DMS, /PMS and /CMS. More addresses can also be provided by using the DSP's flag out pins as a memory select for a peripheral.

Possible 16-bit Peripheral Addresses:

<u>Memory Select</u>	<u>A0 (0 or 1)</u>
/PMS	2 address locations
/DMS	2 “
/IOMS	2 “
/CMS	2 “

8 Total Devices	

Byte Memory Accesses

BDMA accesses are still allowed in Host Mode. However because address pins, A[13:1], became the IAD bus, construction of a complete byte address is impossible. Byte memory addresses on the ADSP-2181 were 22 bit addresses formed from D[23:16] and A[13:0]. In Host Mode D[23:16] and A0 are the only address bits available externally. D[23:16] will be in the DMPAGE register value. A0 will be 1 for odd byte addresses and 0 for even byte addresses. BDMA and IDMA timing and cycle stealing are the same as on the ADSP-2181. BDMA with limited address bits available still provides a flexible interface to the DSP. Without full address bits addressing memory will be more difficult but host or micro-controller communication is possible because the order of the byte sequence is known. For information on byte sequencing, refer to *Byte Memory Word Formats* in chapter 11 of the ADSP-2100 Family User's Manual.